

A Monolithically Integrated 120-GHz InGaAs/InAlAs/InP HEMT Amplifier

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Abstract— We report the design and gain performance for a two-stage 120-GHz monolithically integrated amplifier using 0.1- μm gate length pseudomorphic $\text{In}_{0.60}\text{Ga}_{0.40}\text{As}/\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{InP}$ HEMT's. The two-stage amplifier demonstrated 10–12 dB gain measured between 119.5 to 123.5 GHz. To the best of our knowledge, this is the first demonstration of a monolithically integrated InP HEMT amplifier reported at D-band.

I. INTRODUCTION

DEVELOPMENT of high-performance receivers at D-band (110–170 GHz frequency range) is important for applications in radars, radiometer, remote sensing, and imaging. The potential system advantages with higher frequency operation include higher resolution images, smaller antenna aperture, better compactness, lower power, and lighter weight. InGaAs/InAlAs/InP High Electron Mobility Transistors (InP HEMTs) have demonstrated the best gain and noise performance on a discrete device level at millimeter-wave frequencies due to its intrinsic material properties [1]–[4]. Single-stage and two-stage hybridly integrated InP HEMT amplifiers at 140 GHz have demonstrated 7.3 and 9.3 dB gain, respectively [1]. Here, we report the gain characteristics of a monolithic two-stage 120-GHz amplifier using 0.1- μm gate length pseudomorphic $\text{In}_{0.60}\text{Ga}_{0.40}\text{As}/\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{InP}$ HEMT (PM InP HEMT) technology.

The PM InP HEMT structure [1] is grown using molecular beam epitaxy on a 2-inch InP substrate. Details on device design considerations have been presented elsewhere [5]. For operation at very high frequencies, particular attention was paid to minimize device parasitic capacitances and resistances. Discrete 0.1- μm gate length PM InP HEMT has demonstrated transconductances of 1400 mS/mm, cutoff frequencies of 240 GHz, and maximum oscillation frequencies of 400 GHz at a drain bias of 1 V. A measured gain of 12.2 dB at 94 GHz and 7.3 dB at 140 GHz [2] were obtained from hybrid amplifiers using these devices, which give more validity to the extrapolated f_T and f_{max} numbers. We have also demonstrated a monolithically integrated 75–110 GHz 4-stage balanced InP HEMT amplifier with 23 ± 3 -dB gain across the entire band [6].

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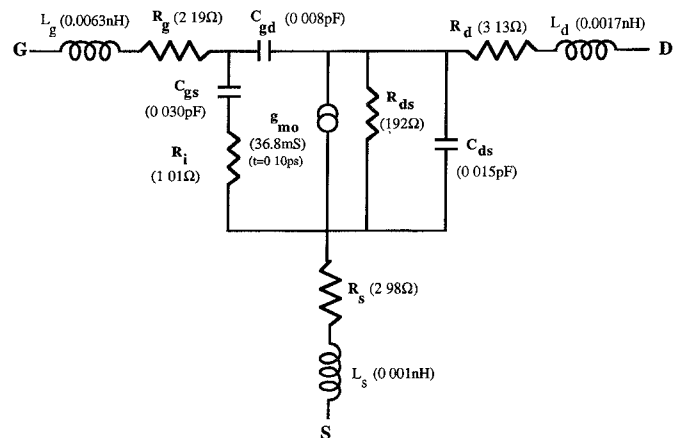


Fig. 1. Equivalent circuit of 0.1- $\mu\text{m} \times 40\text{-}\mu\text{m}$ PM InP HEMT biased at 1.0 V drain bias and 70% I_{ds} at peak G_m .

II. CIRCUIT DESIGN AND PERFORMANCE

The linear small signal model for a 0.1- μm gate length four finger, 40- μm gate width PM InP HEMT [1], [2] used in this 120-GHz LNA design are obtained from the measured small signal S -parameters up to 50 GHz using standard curve fitting techniques. The noise model parameters are also obtained using curve fitting techniques from the measured noise parameters up to 26 GHz. The resulting parameters are consistent with the estimated values based on device physical dimensions and parameters.

The D-band amplifier is a two-stage single-ended design and each stage uses a 40- μm PM InP HEMT (Fig. 1). The input and interstage matching networks are designed for low noise performance and are constructed by cascading high-low impedance microstrip lines. Edge coupled lines are used for dc blocking and radial stubs are employed for RF bypass. Shunt N^+ bulk resistors are included in the bias networks for amplifier stability. The InP substrate was thinned to 70 μm and a wet chemical etching process is used to fabricate back side via holes for grounding. The 70- μm substrate thickness was chosen to minimize the wet etched via hole size, which minimizes the source inductance of the device.

For the 120-GHz amplifier development, a design procedure using full-wave EM analysis for the passive structures to eliminate the uncertainties due to quasi-static models was incorporated in this 120-GHz monolithic amplifier development. The design/analysis methodology, together with the device modeling procedure, was documented in a previous paper

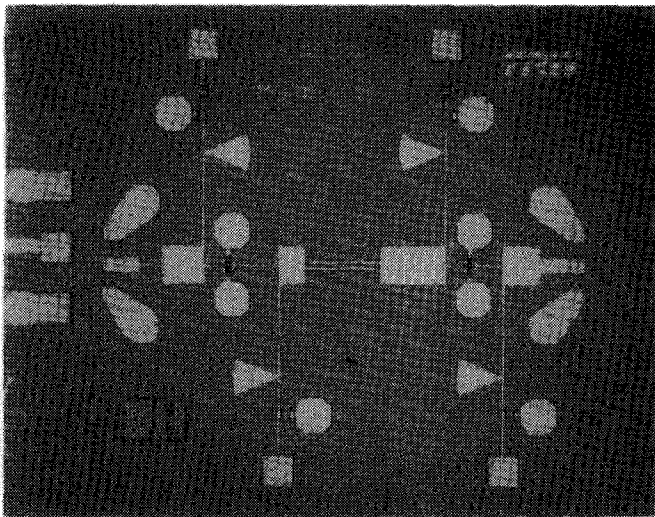


Fig. 2. Photograph of the 2-stage 120-GHz PM InPHEMT MMIC amplifier with a total chip size of $1.7 \times 1.6 \text{ mm}^2$.

[8]. A picture of the 120-GHz amplifier with a total chip size of $1.7 \times 1.6 \text{ mm}^2$ is shown in Fig. 2. The circuit was first tested on-wafer from 100–120 GHz using a verified W-Band on-wafer probe test set [9] for a quick evaluation of the circuit. The measured gain was 8–12 dB from 100–118 GHz. The chip was then tested from 118–125 GHz in a D-band test fixture. Finline waveguide to microstrip transitions were fabricated on 3-mil quartz substrates. The measured insertion loss for a pair of back-to-back transitions was 2 dB at 120 GHz with a return loss $>15 \text{ dB}$. The amplifier's measured gain characteristics are shown in Fig. 3. The amplifier demonstrates 10–12 dB gain from 119.5–123.5 GHz after correction for the transition losses. The measured gain characteristics correspond reasonably well with the simulated results, which show a peak gain of about 11 dB from 118 to 120 GHz. In this study, we were unable to measure the noise performance of the amplifier because verifiable noise measurement systems are not available in this frequency range. The overall DC power dissipation of the circuit was only 42 mW ($V_d = 1.4 \text{ V}$, $I_{d\text{total}} = 30 \text{ mA}$).

III. SUMMARY

We have successfully demonstrated a monolithic D-band two-stage amplifier using $0.1\text{-}\mu\text{m}$ gate length pseudomorphic $\text{In}_{0.60}\text{Ga}_{0.40}\text{As}/\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{InP}$ HEMT technology. The amplifier tested in a D-band fixture showed a measured gain of 10–12 dB from 119.5 to 123.5 GHz. This is believed to be the highest frequency monolithic amplifier ever reported.

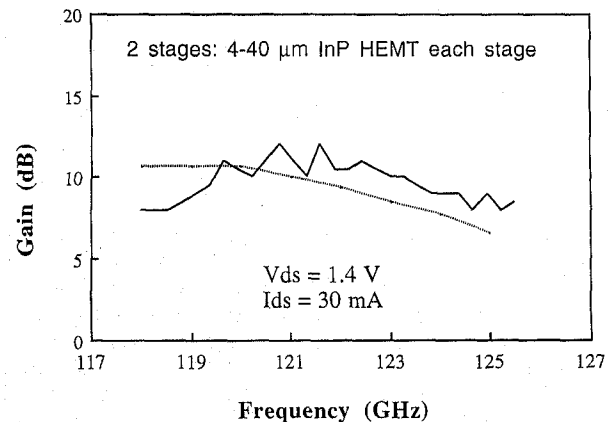


Fig. 3. Measured gain characteristics for the 2-stage 120-GHz amplifier with $V_d = 1.4 \text{ V}$ and $I_d = 30 \text{ mA}$.

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